A Novel Technology for Single Phase Clock Distribution Using VLSI

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Abstract- Frequency synthesizer is one of the important elements for wireless communication application. The speed of VCO and prescaler determines how fast the frequency synthesizer is. A dual modulus prescaler contains logic gates and flip-flops. This project aim for developing a low power single clock multiband network which will supply for the multi clock domain. In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodal's 32/33/47/48 prescaler. Since the multimodal's 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S counters can actually be programmed to divide over the whole range of frequencies. However, the P and S counters are programmed accordingly. The proposed multiband flexible divider also uses an proved loadable bit-cell for Swallow - counter and consumes a power of 0.96 and 2.2 mW, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

Keywords: prescaler, nor gates, multiplexers.

1.INTRODUCTION

Frequency division is one of the important applications of flip-flops. A wide-band frequency synthesizer implemented by phase-locked loop (PLL) uses prescaler (also called N/N+1 counter) as fundamental block. In PLL high frequency output of VCO is coupled directly to the prescaler directly. As process technology is reducing, channel length and supply voltage is decreasing rapidly. Therefore prescaler has to work at high frequency as well as low operating voltage. Due to incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected by creating another propagation delay and the increases the switching power. Since flip-flop works as a part of the clock network, it consumes 30-50% of chip energy. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer uses an E-TSPC prescaler as the most critical blocks in frequency synthesizer because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption.

Division operation is very important in the computer system. For division algorithm earlier they used Phased Lock loop (PLL), but now a day’s we are using hardware module divider. There are so many techniques to implement the divider. In synchronous technique it always need clock signal to trigger the system. If we use this technique we may cause some problems like clock skew, dynamic power consumption etc. But in asynchronous circuits no need of system clock signals so it doesn’t have the shortcomings mentioned above.

The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25 mW in CMOS realizations but it consumes large chip area and has a narrow locking range. To overcome this we used the best published frequency synthesizer at 5 GHz but it consumes power around 9.7 mW. In order to overcome this we used dynamic latches, which are faster and consume less power compared to static divider. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problems. But E-TSPC prescaler will consume 6.25 mW. To overcome this we used a low power wideband 2/3 prescaler and wideband multimodulus 32/33/47/48 prescaler which can consume power up to 158.43 mW. Frequency dividers are also called prescaler which are used in many communication applications like frequency synthesizer, timing-recovery circuits and clock generation circuits. A prescaler is loaded at the feedback path of the synthesizer, takes signal and generates a periodic output signal and frequency. It is one of the most critical blocks in frequency synthesizer because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption.

Fig 1: Proposed Dynamic Logic Multiband Flexible Divider

The frequency synthesizer uses an E-TSPC prescaler as the First-stage divider, but the divider consumes around 6.25 mW. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a Dynamic logic multiband flexible integer-n divider based on pulse-
swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler as shown in Fig.1 The divider also uses an improved low power loadable bit-cell for the Swallow S-counter, a true single-phase-clock (TSPC) policy was introduced. Single-phase-clock policies are superior to the others due to the simplification of the clock distribution on the chip and reducing the transistor number. They reduce the number of clock-signal requirements and the wiring costs also they have no problems with phase overlapping. Thus, higher frequencies and simpler designs can be achieved. Further enhancement in the design is achieved by using extended true-single phase clock (ETSPC) DFFs.

II LITERATURE SURVEY

Title: Wind turbine driven self excited induction generator, H.R.Rategh et al., “A CMOS frequency synthesizer with an injected locked frequency divider for 5GHz wireless LAN receiver. This high power consumption is mainly due to the first stages of the frequency divider that often dissipates half of the total power. Due to the high input frequency, the first stage of the divider cannot be implemented in conventional static CMOS logic. Instead, it is commonly realized in source-coupled logic (SCL), which allows higher operating frequency, but burns more power. A more efficient alternative to the first SCL divider is the injection locking -divider employed in. However, this resonant divider requires a tank whose area is larger than the oscillator’s tank, and it suffers from pulling phenomena.

L. Lai Kan Leung, “A 1-V 9.7-mW CMOS frequency synthesizer for IEEE 802.11a transceivers. High speed divide – by - counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide – by - counter consists of flip - flops (FF) and extra logic, which determines the terminal count. Conventional high speed FF based divide by counter designs use current - mode logic (CML) latches and suffer from the disadvantage of large load capacitance.

V. K. Manthena etc all, “A low power fully programmable J MHz resolution 2.4 GHz CMOS PLL frequency synthesizer. Integrated phased array systems are for the most part too different from normal single channel transceivers. The key additional component is the phase shifter. A new phased array architecture that uses digital phase locked loop PLL modulator to realize phase shift is developed. To achieve phase shifting capability, PLL is a natural candidate. If we combine PLL’s phase shifting and modulation capabilities then we can realize phased array system using solely PLLs. With recent breakthrough in digital PLL, a digital PLL can generate a precise and well-controlled phase shift that analog PLLs cannot. The same phase shift capabilities can be used for data modulation. With both phase shift and data modulation capabilities, we only need an array of such PLLs to realize a phased array. Compared with conventional phased arrays, PLL based phased array can achieve more precise phase shift thus more precise radiation angle. It is also more flexible, since all channels can generate independent phase shift. The adoption of dynamic dividers in CMOS phasedlocked loops for multigigahertz applications allows to reduce the power consumption substantially without impairing the phase noise and the power supply sensitivity of the phase-locked loop (PLL). A 5-GHz frequency synthesizer integrated in a 0.25-μm CMOS technology demonstrates a total power consumption of 13.5 mW. The frequency divider combines the conventional and the extended true-single-phase-clock logics. The oscillator employs a rail-to-rail topology in order to ensure a proper divider function. This PLL intended for wireless LAN applications can synthesize frequencies between 5.14 and 5.70 GHz in steps of 20 MHz. A lowpower 5-GHz CMOS frequency synthesizer for wireless LAN transceivers has been presented. The PLL integrated in a 0.25- m CMOS technology consumes only 13.5 mW, thanks to a dynamic TSPC divider. This class of dividers is demonstrated to be suitable for multigigahertz synthesizers, since it does not impair the power supply rejection or the phase noise performance. WIRELESS LAN systems in the 5–6-GHz band, such as HiperLAN II and IEEE 802.11a, are recognized as the leading standards for high-rate data transmissions. Being intended for mobile operations, the radio transceiver has a limited power budget. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the most critical blocks in terms of average current dissipation since it operates extensively for both receiving and transmitting. The best published integrated synthesizers around 5 GHz suitable for wireless LAN receivers consume up to 25mWin both CMOS and bipolar realizations. Other synthesizers embedded in 802.11a-compliant transceivers can consume up to 200 mW. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in and consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. Frequency synthesizer at 5 GHz consumes 9.7 mW 1-V supply, where its complete divider consumes power around 6 mW where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power.

![Fig 2: Proposed Multimodulus 32/33/47/48 Prescaler](image)

III. RELATED WORK
For a sequential circuit to operate correctly, the processing of data must occur in an orderly fashion. In a synchronous system, the order in which data are processed is coordinated by a clock signal. (To be more general, the synchronization could be performed by a collection of globally distributed clock signals). The clock signal, in the form of a periodic square wave that is globally distributed to control all sequential elements (ip-ops or latches), achieves synchronization of the circuit operation when all data are allowed to pass through the sequential elements simultaneously. A clock network is required to deliver the clock signal to all sequential elements. As the distributive nature of long interconnects becomes more pronounced because of technology scaling, the control of arrival times of the same clock edge at different sequential elements, which are scattered over the entire chip, becomes more difficult. If not properly controlled, the clock skew, denoted as the difference in the clock signal delays to sequential elements, can adversely affect the performance of the systems and even cause erratic operations of the systems (e.g., latching of an incorrect signal within a sequential element).

The design of a clock poses a formidable challenge because of stringent requirements. A well-designed clock must also account for variations in device and interconnect parameters. What complicates matters even further is the interplay between the clock network and the power/ground network. For example, in a zero-skew clock network, all sequential elements are triggered almost simultaneously. Because these elements draw current from the power network or sink current to the ground network almost simultaneously when the clock switches, the zero-skew design often leads to severe power supply noise, resulting in unacceptable degradation in performance and reliability. On the other hand, power supply noise affects the clock jitter (this refers to the time shift in the clock pulse, as well as the variations in the pulse width that arise from the time-varying operating conditions such as supply voltage), which, in turn, affects the arrival times of clock signal at different sequential elements.

Currently, a digital (and electrical) clock signal is distributed using metallic interconnects (e.g., Cu) throughout the entire die. There are many approaches to distribute digital clock signals, such as H-trees, grids, and some combinations of them. In this project, we will consider burred H-trees driving local grids as representative of present clock distribution, to which we will refer as the conventional approach. Advanced active de-skewing techniques, which further improve the quality of standard clock distribution, are not considered in this simple analysis.

Several interconnect solutions have been proposed to mitigate the increasingly difficult clock distribution, 3-D, optical, and RF being the most important ones. 3-D interconnects, which refers to two or more active Si strata that are integrated together (for example by bonding), take advantage of the vertical dimension to decrease the die size, therefore alleviating clock distribution. Optical interconnects have also been proposed for clock distribution since they are immune to crosstalk noise from adjacent electrical interconnects, and because of their speed-of-light propagation. Optical interconnects also have the potential for large bandwidths, which are mostly relevant for signaling. RF approaches using Cu interconnects have been proposed as a low-power clock distribution alternative at the package level. The main difference between the RF approach and conventional approach is that RF uses a narrow-band sinusoidal wave for transmitting the clock signal as opposed to the digital square signal that is employed in conventional clock distribution. An interesting wireless RF clock distribution, in which the clock signal is broadcast by a source and received by on-die antennae, has also been proposed and investigated in. This technique is attractive since it does not require interconnects. However, noise considerations as well as the size and position of the antennae are technical and cost issues that have to be addressed. Most of the benchmarking research has been condensed to global clock distribution. However, in order to truly assess the overall benefits of alternative clock distribution approaches, it is also important to include the local clock distribution in the analysis.

There are many issues to consider in the design of a clock generator. Both power dissipation and jitter play a major role in determining the type of generation system to utilize. Obviously, operating frequency also plays a major role, especially in the present day systems. The large discrepancy between system clock frequency and processor clock frequency inevitably results in the need for a phase-locked loop (PLL) clock generator.

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These important advantages to PLL clock generation do not come without a price. A PLL, unless designed completely from digital circuitry, is essentially an analog circuit, and requires very careful design. The noise inherent in a digital system, especially a high-speed microprocessor, can cause many problems for a PLL clock generator. Furthermore, PLLs typically require relatively large passive elements for stable operation. Some integrated circuit technologies do not lend themselves well to the creation of such structures. Last, but certainly not least, even a well-designed PLL exhibits variation in its output phase and frequency over time.

The components of a PLL that are most susceptible to noise are the phase detector, charge pump, and voltage-controlled oscillator (VCO). With careful layout and circuit design the jitter due to noise in the phase detector and charge pump can be largely eliminated, but the VCO is a very sensitive circuit that bears closer inspection.
IV METHODOLOGY

The single-phase clock multiband flexible divider which is shown in Fig consists of the multi modulus 64/65 prescaler, a 7-bit programmable P-counter and a 6 bit swallow Scounter. The control signal MODE decides whether the divider is operating in lower frequency band or higher band. A. Swallow (S) Counter: The 6 bit s counter shown in fig.5 consist of six asynchronous loadable bit cells, a NOR embedded DFF and additional logic gates. If MOD is logically high nodes s1 and s2 switches to logic 0 and the bit cell does not perform any function. The MOD signal goes logically high only when the s-counter finishes counting down to zero.

In the initial state, MOD=0, multimodulus prescaler selects the divide by (N) mode and p, S counter start down counting the input clock cycles. When the s counter finishes counting, MOD switches to logic 1 and the prescaler changes to divide by N+1 mode for the remaining clock cycles. B. Programmable (P) Counter: The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band.

When the P-counter finishes counting down to zero, LD switches to logic “1” during which the output of all the bit-cells in S-counter switches to logic “1” and output of the NOR embedded DFF switches to logic “0” (MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 64 (N) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band (5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus 64/65 prescaler eases the design complexity of the P-counter.

IV. RESULTS

Simulated Environment

Fig. 3: Asynchronous 6-bit counter

Fig. 4 Simulation Result

Fig. 5 Simulation Result
IV. CONCLUSION

In this paper, a multiband flexible divider is implemented which consist of a consist of program counter; swallow s counter and multimodulus prescaler. It is simulated by using modalism 6.4c. This type of divider is widely used in Bluetooth, Zigbee technologies which are the common wireless standards. A modified divider is also implemented in this paper by integrating p and s counters in the existing system to achieve high performance, to simplify the circuit etc. Also in the modified flexible divider existing 2/3 prescaler is replaced with modified 4/5 prescaler. By the implementation of modified divider we can achieve reduced power consumption

REFERENCE


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